FORM PTO-1390 (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY DOCKET NUMBER	U.S. APPLICATION NO. (If known, see 37 CFR 1.5)
232.001	09/720953

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP99/03664	07 July 1999	08 July 1998

TITLE OF INVENTION *Printed Circuit Board and Method of Manufacturing Same*

APPLICANT(S) FOR DO/EO/US Kiyotaka TSUKADA, Masaru TAKADA, and Kenji CHIHARA

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371 (f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371 (b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371 (c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C.371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 11. To 16. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98. (and references)
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment including a *Request to Approve Drawing Change*.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information:

A copy of the WIPO Publication (WO 00/03572) and International Search Report; Form PCT/IB/304; Form PCT/IB/308; and Form PCT/IB/332, are also enclosed.

U.S. APPLICATION NO (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY DOCKET NUMBER
09/720953	PCT/JP99/03664	232.001

17. ☒ The following fees are submitted:

CALCULATIONS PTO USE ONLY

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1000.00**

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO. **$860.00**

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445 (a)(2)) paid to USPTO **$710.00**

International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**

International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33 (1)-(4). **$100.00**

ENTER APPROPRIATE BASIC FEE AMOUNT =				$ 860.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).				$ 0.00	
Total claims	13 - 20 =	0	X **$18.00**	$ 0.00	
Independent claims	3- 3 =	0	X **$80.00**	$ 0.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$270.00**	$ 0.00	
TOTAL OF ABOVE CALCULATIONS =				$ 860.00	
Reduction of ½ for filing by small entity, if applicable. A Small Entity Statement must also be filed (Note 37 CFR 1.9,1.27, 1.28).				$ 0.00	
SUBTOTAL =				$ 860.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).			+	$ 0.00	
TOTAL NATIONAL FEE =				$ 860.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property			+	$ 40.00	
TOTAL FEES ENCLOSED =				$ 900.00	
				Amount to be: Refunded	$
				Charged	

a. ☒ A check in the amount of $ 900.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. 50-1170 in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-1170. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO
BOYLE FREDRICKSON NEWHOLM STEIN & GRATZ S.C
250 East Wisconsin Avenue, Suite 1030
Milwaukee, WI 53202-4232
Telephone (414) 225-9755
Facsimile (414) 225-9753

SIGNATURE:

James F. Boyle

NAME

33,653 — REGISTRATION NUMBER

January 3, 2001 — DATE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Tsukada, et al. Atty. Docket No. 232.001

Serial No.: (unassigned) Group: (unassigned)

Filing Date: Examiner: (unassigned)

Title: ***Printed Circuit Board and Method of Manufacturing Same***

Priority: PCT/JP99/03664; Filed July 7, 1999

PRELIMINARY AMENDMENT

DO/EO/US
Director of the U.S. Patent and Trademark Office
Washington, DC 20231

Dear Sir:

This Preliminary Amendment is directed to a new U.S. application as identified above. Please enter this preliminary amendment prior to calculating the fees.

IN THE SPECIFICATION:

Page 1, line 1, delete "SPECIFICATION";

line 5, delete "TECHNICAL FIELD" and insert therefor --BACKGROUND OF THE INVENTION--; and line 12, delete "BACKGROUND ART".

Page 7, line 5, delete "BEST MODE FOR CARRYING OUT" and insert therefor --DETAILED DESCRIPTION OF--.

IN THE CLAIMS (As Amended to Incorporate the Article 34 Amendments):

Please amend claims 1-8, as follows:

1. (Amended) A method for manufacturing a printed circuit board [characterized by] comprising the steps of:

coating a lower surface and an upper surface of an insulative substrate respectively with a lower surface metal foil and an upper surface metal foil, the thickness of which is less than that of the lower surface metal foil;

forming an opening in the upper surface metal foil at a location corresponding to a blind via hole formation portion of the insulative substrate;

forming a blind via hole, the bottom of which is the lower surface metal foil, by emitting a laser against the blind via hole formation portion through the opening;

applying a conductor to the blind via hole; and

forming an upper surface pattern and a lower surface pattern by respectively etching the upper surface metal foil and the lower surface metal foil.

2. (Amended) A method for manufacturing a printed circuit board [characterized by] comprising the steps of:

coating a lower surface and an upper surface of an insulative substrate respectively with a lower surface metal foil and an upper surface metal foil, the thickness of which is less than that of the lower surface metal foil;

forming an upper surface pattern and a lower surface pattern by respectively etching the upper surface metal foil and the lower surface metal foil, wherein the upper surface pattern has an opening exposing the upper surface of the insulative substrate at a location corresponding to a

blind via hole formation portion, and the lower surface pattern covers the lower surface of the insulative substrate at a location corresponding to the blind via hole formation portion;

forming a blind via hole, the bottom of which is the lower surface pattern, by emitting a laser against the insulative substrate through the opening; and

applying a conductor to the blind via hole.

3. (Amended) The printed circuit board manufacturing method according to claim 1 [or 2], [characterized in that] wherein the upper surface and lower surface metal foil coating step includes a step of coating the upper surface and the lower surface, respectively, with an upper surface metal foil and a lower surface metal foil that have the same thickness, and a step for etching the upper surface metal foil.

4. (Amended) The printed circuit board manufacturing method according to claim 1 [or 2], [characterized in that] wherein the upper surface and lower surface metal foil coating step includes a step for coating the upper surface and the lower surface, respectively, with an upper surface metal foil and a lower surface metal foil that have the same thickness, and a step for further coating the lower surface metal foil with a metal plating film.

5. (Amended) The printed circuit board manufacturing method according to claim 1 [or 2], [characterized in that] wherein the upper surface and lower surface metal foil coating step includes a step for coating the upper surface and the lower surface, respectively, with an upper surface metal foil and a lower surface metal foil that have the same thickness, and a step for

performing a sandblast treatment to the upper surface metal foil so that the thickness of the upper surface metal foil becomes less that of the lower surface metal foil.

6. (Amended) The printed circuit board manufacturing method according to claim 1 [or 2], [characterized in that] wherein the thickness of the upper surface pattern is 2 to 12 μm.

7. (Amended) The printed circuit board manufacturing method according to claim 1 [or 2], [characterized in that] wherein the thickness of the lower surface pattern is 15 to 25μm.

8. (Amended) A printed circuit board [characterized by] comprising:

an insulative substrate;

an upper surface pattern and a lower surface pattern provided, respectively, on an upper surface and a lower surface of the insulative substrate; and

a blind via hole for electrically connecting the upper surface pattern and the lower surface pattern, wherein an upper portion of the blind via hole is opened and a bottom of the blind via hole is covered by the lower surface pattern, the thickness of the upper surface pattern being less than that of the lower surface pattern.

Please add claims 9-13, as follows:

9. (New) The printed circuit board manufacturing method according to claim 2, wherein the upper surface and lower surface metal foil coating step includes a step of coating the upper surface and the lower surface, respectively, with an upper surface metal foil and a lower surface metal foil that have the same thickness, and a step for etching the upper surface metal foil.

10. (New) The printed circuit board manufacturing method according to claim 2, wherein the upper surface and lower surface metal foil coating step includes a step for coating the upper surface and the lower surface, respectively, with an upper surface metal foil and a lower surface metal foil that have the same thickness, and a step for further coating the lower surface metal foil with a metal plating film.

11. (New) The printed circuit board manufacturing method according to claim 2, wherein the upper surface and lower surface metal foil coating step includes a step for coating the upper surface and the lower surface, respectively, with an upper surface metal foil and a lower surface metal foil that have the same thickness, and a step for performing a sandblast treatment to the upper surface metal foil so that the thickness of the upper surface metal foil becomes less that of the lower surface metal foil.

12. (New) The printed circuit board manufacturing method according to claim 2, wherein the thickness of the upper surface pattern is 2 to 12μm.

13. (New) The printed circuit board manufacturing method according to claim 2, wherein the thickness of the lower surface pattern is 15 to 25μm.

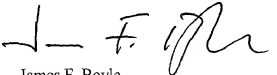
IN THE DRAWINGS:

Amend Figs. 4(a), 4(b) and 4(x) to include the legend -(Prior Art)--, as indicated in red on the attached copies of Figs. 4(a), 4(b) and 4(x).

REMARKS

Claims 1-13 are active in the present application. This application has been amended to insert headings in t he specification, to eliminate the multiple dependencies in the claims, to incorporate Article 34 Amendments from the corresponding PCT application and to amend the Figs. 4(a), 4(b) and 4(x). Entry of the amendments and early consideration and allowance are respectfully requested.

Respectfully submitted,



James F. Boyle
Registration No. 33,653

Dated: January 3, 2001

BOYLE FREDRICKSON NEWHOLM
STEIN & GRATZ S.C.
250 Plaza, Suite 1030
150 East Wisconsin Avenue
Milwaukee, WI 53202
Telephone: (414) 225-9755
Facsimile: (414) 225-9753

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Tsukada, et al.	Atty.	Docket No. 232.001
Serial No.:	(unassigned)	Group:	(unassigned)
Filing Date:		Examiner:	(unassigned)

Title: ***Printed Circuit Board and Method of Manufacturing Same***

Priority: PCT/JP99/03664; Filed July 7, 1999

REQUEST TO APPROVE DRAWING CHANGE

Director of the U.S. Patent
and Trademark Office
Washington, D.C. 20231

Sir:

Applicant submits herewith one sheet of drawings with red ink markings showing the proposed changes to Figs. 4(a), 4(b) and 4(s) for which the approval of the Examiner is requested. The drawing is amended to include the legend "Prior Art" as discussed at page 5 of the Preliminary Amendment filed herewith. Upon the Examiner's approval and allowance of this application, applicant will submit formal drawings incorporating the proposed changes.

Respectfully submitted

James F. Boyle
Registration No. 33,653

Dated: January 3, 2001

BOYLE FREDRICKSON NEWHOLM
STEIN & GRATZ S.C.
250 Plaza, Suite 1030
250 East Wisconsin Avenue
Milwaukee, WI 53202
Telephone: (414) 225-9755
Facsimile: (414) 225-9753

{00001441.DOC /}

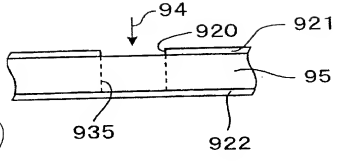


Fig. 4(a)
(Prior Art)

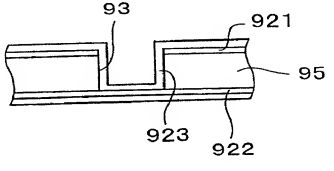


Fig. 4(b)
(Prior Art)

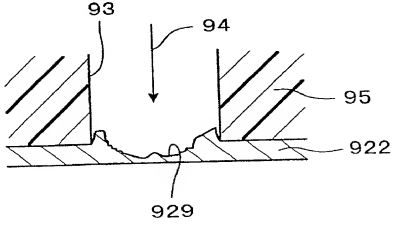


Fig. 4(x)
(Prior Art)

SPECIFICATION

PRINTED CIRCUIT BOARD AND METHOD OF MANUFACTURING SAME

TECHNICAL FIELD

The present invention relates to a printed circuit board and a method of manufacturing same, and more particularly, to the formation of a pattern and the formation of a blind via hole on a printed circuit board.

BACKGROUND ART

In the prior art, a printed circuit board includes an insulative substrate having an upper surface on which an upper surface pattern is formed and a lower surface on which a lower surface pattern is formed, and blind via holes for electrically connecting the upper and lower surface patterns. Due to the recent trend of greater integration, a blind via hole is formed by a laser so that it has a microscopic diameter.

To form a blind via hole with a laser, as shown in Fig. 4(a), an upper surface and a lower surface of an insulative substrate 95 are respectively coated by upper surface and lower surface metal foils 921, 922. An opening 920 is formed in the upper surface metal foil 921 in correspondence with a blind via hole formation portion 935, and a laser 94 is emitted toward the opening 920. The laser 94 forms an opening in the insulative substrate 95 at a position corresponding to the blind via hole formation portion 935 and forms a blind via hole 93 that extends to the lower

surface metal foil 922. As shown in Fig. 4(b), after the formation of the blind via hole 93 is completed, chemical plating or electroplating is performed to form a metal plating film 923 on the wall of the blind via hole 93.

However, since the metal foil is thick in the conventional printed circuit board, etching must be performed under severe conditions, and etching takes time. Thus, the formation of the upper surface pattern through etching is difficult. This decreases work efficiency.

Accordingly, the thickness of the metal foil may be reduced. However, in this case, as shown in Fig. 4(x), the thickness of the lower surface metal foil 922 is reduced, the laser 94 may inflict damage 929 on the lower surface metal foil 922.

It is an object of the present invention to provide a printed circuit board and method of manufacturing same that facilitate the formation of the upper surface pattern and prevent a laser from damaging the lower metal foil when forming blind via holes.

SUMMARY OF THE INVENTION

A first embodiment according to the present invention proposes a method for manufacturing a printed circuit board. The method includes the steps of coating a lower surface and an upper surface of an insulative substrate, respectively, with a lower surface metal foil and an upper surface metal foil, the thickness of which is less than that of the lower surface metal foil, forming an opening in the upper surface

metal foil at a portion corresponding to a blind via hole formation portion of the insulative substrate, forming a blind via hole, the bottom of which is the lower surface metal foil, by emitting a laser against the blind via hole formation portion through the opening, applying a conductor to the blind via hole, and forming an upper surface pattern and a lower surface pattern by respectively etching the upper surface metal foil and the lower surface metal foil.

The thickness of the upper surface metal foil is less than the thickness of the lower surface metal foil. This facilitates etching of the upper surface pattern, and the thickness of the lower surface metal foil is such that the lower surface metal foil is prevented from being damaged by the emission of a laser during formation of the blind via hole. Accordingly, the upper pattern is easily formed through etching, damage to the lower surface pattern due to the laser emission is prevented, and a conductor is applied to the blind via hole in a satisfactory state.

When making the upper surface metal foil thinner than the lower surface metal foil, after both surfaces of the insulative substrate are respectively coated with an upper surface metal foil and a lower surface metal foil that have the same thickness, it is preferred that etching be performed on the upper surface metal foil to remove part of the upper surface metal foil. In this manner, by performing etching in a single step, the formation of the thin upper surface metal foil is facilitated.

Alternatively, when making the upper surface metal foil thinner than the lower surface metal foil, after both

surfaces of the insulative substrate are respectively coated with an upper surface metal foil and a lower surface metal foil that have the same thickness, a metal plating film may further be applied to the surface of the lower metal foil.

It is preferred that the thickness of the upper surface pattern be 2 to 12μm. When thinner than 2μm, the strength of the upper pattern may be insufficient. When thicker than 12μm, etching may be difficult during the formation of the upper surface pattern.

It is preferred that the thickness of the lower surface pattern be 15 to 25μm. When thinner than 15μm, the lower surface pattern, which defines the bottom of the blind via hole, may be damaged by the laser emission. Further, there is no benefit to making the thickness greater than 25μm.

To apply a conductor to the via hole, for example, chemical plating and electroplating may be performed to form a metal plating film on the wall of the via hole or the interior of the via hole may be filled with a conductive material, such as solder. However, other methods may be employed to apply a conductor.

A resin material, such as epoxy, polyimide, and bismaleimidetriazine, or a filler-containing multiple resin substrate made of these resin materials in addition to glass cloth and glass filler may be used as the insulative substrate.

The upper surface metal foil and the lower surface metal foil may, for example, both be made of copper foil,

although other materials may be used.

In the above manufacturing method, the upper surface pattern and the lower surface pattern are formed after applying a conductor to the blind via hole. However, the upper surface pattern and the lower surface pattern may be formed before forming the blind via hole.

That is, in a second embodiment according to the present invention, a method for manufacturing a printed circuit board includes the steps of coating a lower surface and an upper surface of an insulative substrate respectively with a lower surface metal foil and an upper surface metal foil the thickness of which is less than that of the lower surface metal foil and forming an upper surface pattern and a lower surface pattern by respectively etching the upper surface metal foil and the lower surface metal foil. The upper surface pattern has an opening exposing the upper surface of the insulative substrate at a portion corresponding to a blind via hole formation portion. The lower surface pattern covers the lower surface of the insulative substrate at a portion corresponding to the blind via hole formation portion. The method further includes the steps of forming a blind via hole, the bottom of which is the lower surface pattern, by emitting a laser against the insulative substrate through the opening, and applying a conductor to the blind via hole.

The manufacturing method of the second embodiment obtains the same effects as the manufacturing method of the first aspect. The details are the same as the manufacturing method of the first embodiment.

A third embodiment provides a printed circuit board obtained through the manufacturing method of the first or second embodiments. The printed circuit board includes an insulative substrate, an upper surface pattern and a lower surface pattern provided, respectively, on an upper surface and a lower surface of the insulative substrate, and a blind via hole for electrically connecting the upper surface pattern and the lower surface pattern. An upper portion of the blind via hole is opened and a bottom of the blind via hole is covered by the lower surface pattern. The thickness of the upper surface pattern is less than that of the lower surface pattern.

The upper surface pattern is thinner than the lower surface pattern. Thus, when manufacturing the printed circuit board, etching for forming the upper surface pattern is facilitated. Further, the lower surface pattern, which defines the bottom of the blind via hole, is not damaged by the laser emission, and the blind via hole is formed in a satisfactory state.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic cross-sectional view showing a printed circuit board according to an embodiment of the present invention;

Fig. 2 is a schematic cross-sectional view showing a printed circuit board according to an embodiment of the present invention;

Figs. 3(a) to 3(i) are explanatory diagrams illustrating a method for manufacturing a printed circuit board according to an embodiment of the present invention;

and

Fig. 4 is an explanatory view showing a method for manufacturing prior examples of printed circuit boards.

BEST MODE FOR CARRYING OUT THE INVENTION

A printed circuit board according to an embodiment of the present invention will now be described with reference to Figs. 1 to 4.

As shown in Figs. 1 and 2, a printed circuit board 4 includes an insulative substrate 5, an upper surface pattern 21 formed on the upper surface of the insulative substrate 5, a lower surface pattern 22 formed on the lower surface of the insulative substrate 5, and blind via holes 3 electrically connecting the upper surface pattern 21 and the lower surface pattern 22. The upper portions of the blind via holes 3 are opened, and the lower portions of the blind via holes 3 are covered by the lower surface pattern 22.

As shown in Fig. 1, the thickness t of the upper surface pattern 21 is less than the thickness T of the lower surface pattern 22. The difference between the thickness T of the lower surface pattern 22 and the thickness t of the upper surface pattern 21 is substantially the same as the thickness of the plating applied to the blind via holes and is about 3 to 10μm.

The surfaces of the upper surface pattern 21 and the lower surface pattern 22 and the walls of the blind via holes 3 are coated by a metal plating film 23. The surface of the insulative substrate 5, including the interiors of

the blind via holes 3, is coated with a solder resist 55. Connection balls 61, which are connected to an electronic component 71, are adhered to the upper surface pattern 21 via a metal plating film 231. Further, solder balls 6, which are used to arrange the printed circuit board 4 on an external substrate, are adhered to the lower surface pattern 22 via a metal plating film 231.

A method for manufacturing the printed circuit board will now be described.

Referring to Fig. 3(a), a glass epoxy substrate, which is used as the insulative substrate 5, is first prepared. Then, the upper and lower surfaces of the insulative substrate 5 are respectively coated by an upper surface metal foil 210 and a lower surface metal foil 220. The thickness t of the upper surface metal foil 210 is less than the thickness T of the lower surface metal foil 220. It is preferred that the coating of the upper surface metal foil 210 and the lower surface metal foil 220 be substances having thicknesses t and T, respectively. As an alternative example, a surface treatment, such as sandblasting, may be performed to adjust the thickness of the upper surface metal foil so that the thickness t of the upper surface metal foil 210 becomes less than the thickness T of the lower surface metal foil 220. Further, upper surface and lower surface metal foils having the same thickness may be respectively applied to the upper surface and lower surface of the insulative substrate 5, and the upper surface metal foil may be etched until it is reduced to the thickness t to form the upper surface metal foil 210. The upper surface metal foil 210 and the lower surface metal foil 220 are preferably

copper foils.

Then, as shown in Fig. 3(b), a portion of the upper surface metal foil 210 corresponding to a blind via hole formation portion 35 of the insulative substrate 5 is etched to form an opening 213.

Then, a laser 8 is emitted against the surface of the surface of the insulative substrate 5 exposed by the opening 213, or the blind via hole formation portion 35. This forms the blind via hole 3, the bottom of which is the lower surface metal foil 220, as shown in Fig. 3(c).

Then, with reference to Fig. 3(d), a chemical copper plating and an electric copper plating are applied to the wall of the blind via hole 3 to form the metal plating film 23. The surfaces of the upper surface metal foil 210 and the lower surface metal foil 220 are also coated by the metal plating film 23.

Then, with reference to Fig. 3(e), the upper surface metal foil 210 and the lower surface metal foil 220 are etched to form the upper surface pattern 21 and the lower surface pattern 22.

Then, with reference to Fig. 3(f), the solder resist 55 is applied to the upper surface and lower surface of the insulative substrate 5. The solder resist 55 is applied so that a connection ball adhering portion 211 of the upper surface pattern 21 and a solder ball adhering portion 221 of the lower surface pattern 22 are exposed.

Then, as shown in Fig. 3(g), a metal plating film 231, which is formed from nickel and gold, is applied to the connection ball adhering portion 211 of the upper surface pattern 21 and the solder ball adhering portion 221 of the lower surface pattern 22.

Then, as shown in Fig. 3(h), the electronic component 71 is adhered to the connection ball adhering portion 211 of the upper surface pattern 21 by the connection ball 61, which is formed from solder.

Then, as shown in Fig. 3(i), under filling is performed using a filling material 59, such as an epoxy resin.

The printed circuit board 4 of Figs. 1 and 2 is manufactured as described above.

The operation and advantages of the present embodiment will now be discussed.

In the printed circuit board manufacturing method according to the present embodiment, the thickness t of the upper surface metal foil 210 is less than the thickness T of the lower surface metal foil 220. Thus, with reference to Fig. 3(e), this facilitates etching when etching the thin upper surface metal foil 210 to form the upper surface pattern 21. Further, as shown in Fig. 3(b), the thick lower surface metal foil 220 is not damaged by the emission of the laser 8 during formation of the blind via hole.

Accordingly, the manufacturing method of the present embodiment enables the upper surface pattern 21 to be easily

formed through etching. Further, the lower surface pattern 22, which is the bottom of the blind via hole, is prevented from being damaged by the laser emission during formation of the blind via hole, and a conductor is applied to the blind via hole 3 in a satisfactory state.

CLAIMS:

1. A method for manufacturing a printed circuit board characterized by the steps of:

coating a lower surface and an upper surface of an insulative substrate respectively with a lower surface metal foil and a lower surface metal foil, the thickness of which is less than that of the lower surface metal foil;

forming an opening in the upper surface metal foil at a location corresponding to a blind via hole formation portion of the insulative substrate;

forming a blind via hole, the bottom of which is the lower surface metal foil, by emitting a laser against the blind via hole formation portion through the opening;

applying a conductor to the blind via hole; and

forming an upper surface pattern and a lower surface pattern by respectively etching the upper surface metal foil and the lower surface metal foil.

2. A method for manufacturing a printed circuit board characterized by the steps of:

coating a lower surface and an upper surface of an insulative substrate respectively with a lower surface metal foil and an upper surface metal foil, the thickness of which is less than that of the lower surface metal foil;

forming an upper surface pattern and a lower surface pattern by respectively etching the upper surface metal foil and the lower surface metal foil, wherein the upper surface pattern has an opening exposing the upper surface of the insulative substrate at a location corresponding to a blind via hole formation portion, and the lower surface pattern covers the lower surface of the insulative substrate at a

location corresponding to the blind via hole formation portion;

forming a blind via hole, the bottom of which is the lower surface pattern, by emitting a laser against the insulative substrate through the opening; and

applying a conductor to the blind via hole.

3. The printed circuit board manufacturing method according to claim 1 or 2, characterized in that the upper surface and lower surface metal foil coating step includes a step of coating the upper surface and the lower surface, respectively, with an upper surface metal foil and a lower surface metal foil that have the same thickness, and a step for etching the upper surface metal foil.

4. The printed circuit board manufacturing method according to claim 1 or 2, characterized in that the upper surface and lower surface metal foil coating step includes a step for coating the upper surface and the lower surface, respectively, with an upper surface metal foil and a lower surface metal foil that have the same thickness, and a step for further coating the lower surface metal foil with a metal plating film.

5. The printed circuit board manufacturing method according to claim 1 or 2, characterized in that the upper surface and lower surface metal foil coating step includes a step for coating the upper surface and the lower surface, respectively, with an upper surface metal foil and a lower surface metal foil that have the same thickness, and a step for performing a sandblast treatment to the upper surface metal foil so that the thickness of the upper surface metal

foil becomes less that of the lower surface metal foil.

6. The printed circuit board manufacturing method according to claim 1 or 2, characterized in that the thickness of the upper surface pattern is 2 to 12μm.

7. The printed circuit board manufacturing method according to claim 1 or 2, characterized in that the thickness of the lower surface pattern is 15 to 25μm.

8. A printed circuit board characterized by:

an insulative substrate;

an upper surface pattern and a lower surface pattern provided, respectively, on an upper surface and a lower surface of the insulative substrate; and

a blind via hole for electrically connecting the upper surface pattern and the lower surface pattern, wherein an upper portion of the blind via hole is opened and a bottom of the blind via hole is covered by the lower surface pattern, the thickness of the upper surface pattern being less than that of the lower surface pattern.

ABSTRACT

A printed circuit board and a method for manufacturing the same that facilitates the formation of an upper surface pattern and prevents a lower surface metal foil from being damaged when forming a blind via hole with a laser is provided. A lower surface and an upper surface of an insulative substrate (5) are respectively coated with a lower surface metal foil (220) and an upper surface metal foil (210), the thickness of which is less than that of the lower surface metal foil (220). Next, an opening (213) is formed in the upper surface metal foil at a location corresponding to a blind via hole formation portion (35) of the insulative substrate. A blind via hole (3), the bottom of which is the lower surface metal foil, is formed by emitting a laser (8) against the blind via hole formation portion (35) through the opening (213). Then, a metal plating film (23) is applied to the wall of the blind via hole (3), and an upper surface pattern (21) and a lower surface pattern (22) are formed through etching.

Fig. 1

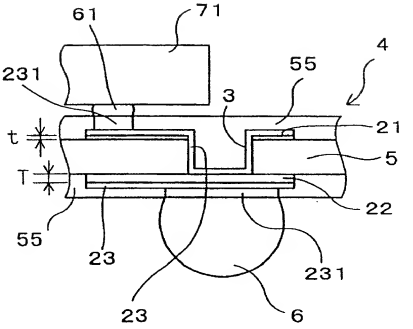


Fig. 2

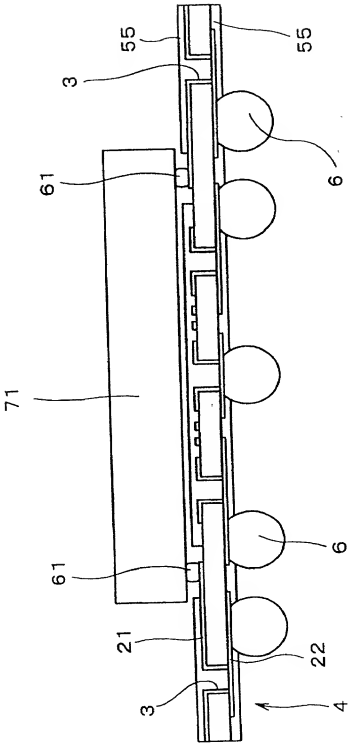


Fig. 3(a)

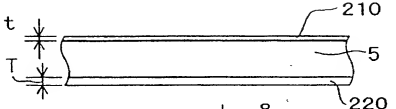


Fig. 3(b)

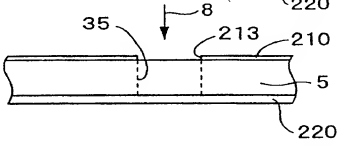


Fig. 3(c)

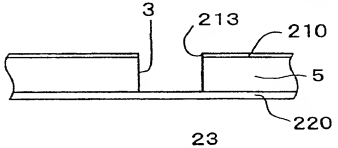


Fig. 3(d)

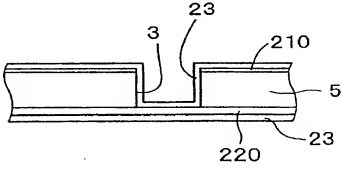


Fig. 3(e)

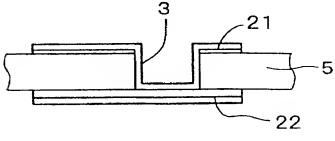


Fig. 3(f)

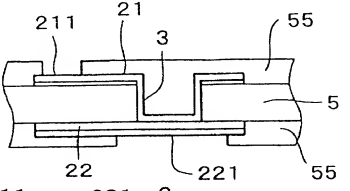


Fig. 3(g)

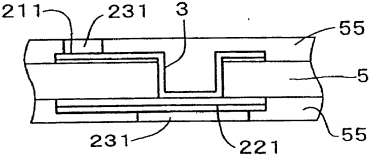


Fig. 3(h)

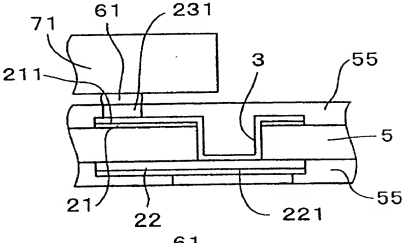


Fig. 3(i)

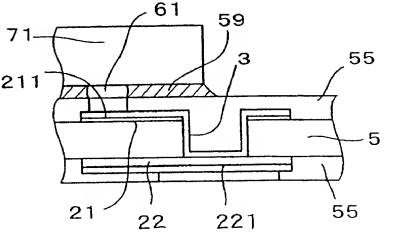


Fig. 4(a)

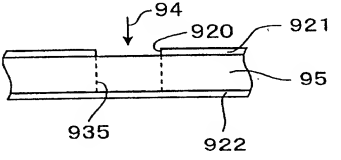


Fig. 4(b)

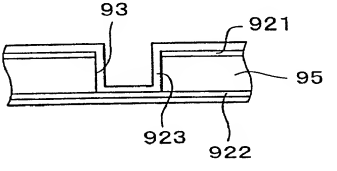
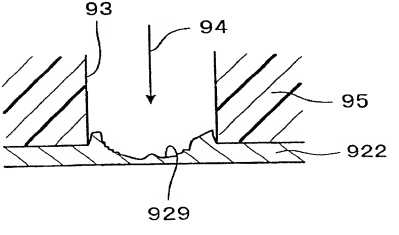


Fig. 4(x)



09/

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled PRINTED CIRCUIT BOARD AND METHOD OF MANUFACTURING SAME, which is described and claimed in

- ☐ the attached specification.
- ☐ the specification in application _____, filed on _____ and amended on _____ (if applicable).
- ☒ international (PCT) application No. PCT/JP99/03664 filed on 07 / 07 / 1999 and as amended on 21 / 04 / 2000 (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is known to be material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s) (Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed
Pat. Appln. No. 10-192992	Japan	08 / 07 / 1998	☒ Yes ☐ No
			☐ Yes ☐ No
			☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is known to be material to the patentability of this application as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT International filing date of this application.

(Application Number)	(Filing Date)	(Status - Patented, Pending, Abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: James F. Boyle, Reg. No. 33,653; Timothy E. Newholm, Reg. No. 34,400; Timothy J. Ziolkowski, Reg. No. 38,368; David D. Stein, Reg. No. 40,828; Michael J. Gratz, Reg. No. 39,693; Matthew M. Eslami, Reg. No. 45,488.

Address all telephone calls to James F. Boyle at telephone number (414) 225-9755, facsimile number (414) 225-9753.

Address all correspondence to: James F. Boyle
BOYLE FREDRICKSON ZIOLKOWSKI S.C.
250 Plaza, Suite 1030
250 East Wisconsin Avenue
Milwaukee, Wisconsin 53202

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor (given name, family name): Kiyotaka TSUKADA

Inventor's signature: Kiyotaka Tsukada Date: December 13, 2000

Residence: Ogaki-shi, Japan Citizenship: Japan

Post Office Address: c/o IBIDEN CO., LTD. 2-1, Kanda-cho, Ogaki-shi, Gifu 503-0917 Japan

Title:

Inventor(s):

Full name of second joint inventor, if any (given name, family name): Masaru TAKADA

Inventor's signature: Masaru Takeda Date: December 13, 2000

Residence: ~~Ogaki-shi,~~ Japan Citizenship: Japan

Post Office Address: c/o IBIDEN CO., LTD. 2-1, Kanda-cho, Ogaki-shi, Gifu 503-0917 Japan

SEE ATTACHED SUPPLEMENTAL SHEET

SUPPLEMENTAL SHEET

ADDITIONAL JOINT INVENTOR

Name: Kenji CHIHARA Citizen of: Japan

Residing at: Ogaki-shi, Japan

Post Office Address: c/o IBIDEN CO., LTD. 2-1, Kanda-cho, Ogaki-shi, Gifu 503-0917 Japan

Signature: Kenji Chihara Date: December 13, 2000